FSC-BT626

4.2 Single Mode Bluetooth Module Data Sheet

Document Type: FSC-BT626

Document Version: V1.1

Release Date: Jun 15，2016

Shenzhen Feasycom Technology Co.,Ltd.

Telephone: 86-755-27924639

www.feasycom.com

Release Record

Version Number	Release Date	Comments
Revision 1.0	2015-10-10	First Release
Revision 1.1	2016-06-15	1 Modify the Pin function definition. 2 Modify the application circuit diagram.

1. INTRODUCTION

FSC-BT626 is a fully integrated Bluetooth module that complies with Bluetooth 4.2 single mode protocols(BLE). It supports GAP, ATT/GATT, SMP, L2CAP profiles. It integrates Baseband controller in a small package(Integrated chip antenna), so the designers can have better flexibilities for the product shapes.

FSC-BT626 can be communicated by UART port. With Feasycom's Bluetooth stack, Customers can easily transplant to their software. Please refer to Feasycom stack design guide.

1.1 Block Diagram

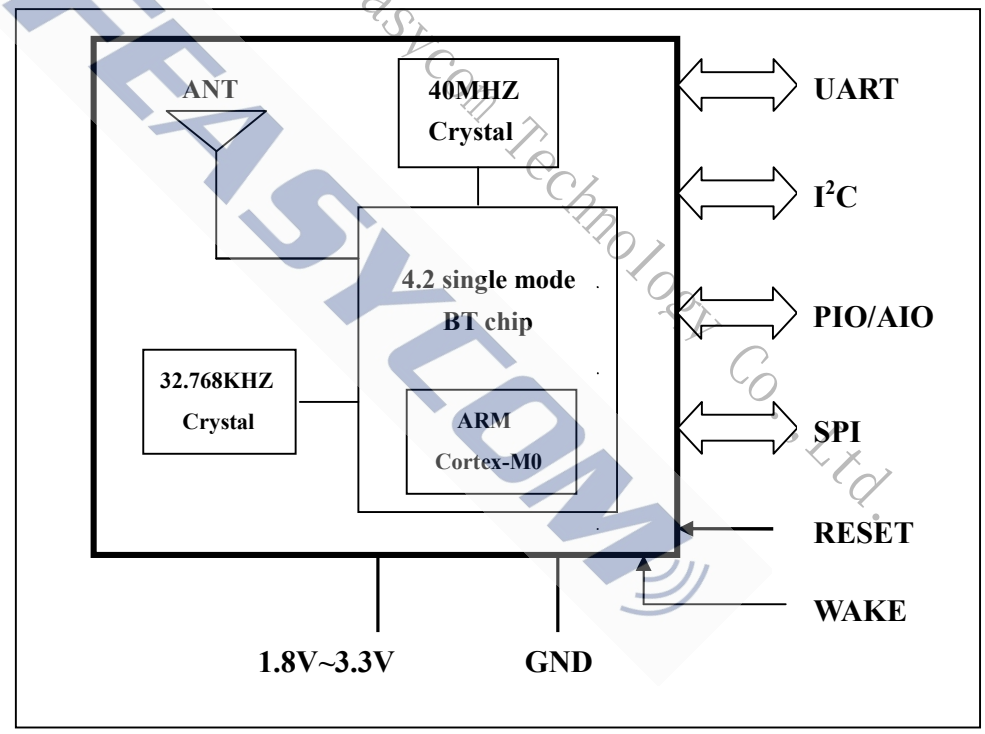

Figure 1

1.2 Feature

- Support the Bluetooth 4.2 core specification.
- Integrate MCU to execute Bluetooth protocol stack.
- Postage stamp sized form factor.
- Low power.
- Class 1.5 support(high output power)
- The default UART Baud rate is 115.2Kbps and can support from 1200bps up to 921Kbps,.
- UART, I^2C,SPI data connection interfaces.
- Support the OTA upgrade.
- Bluetooth stack profiles support: LE HID, and all BLE protocols.

1.3 Application

- Smart Watch and Bluetooth Bracelet
- Health & Medical devices
- TV Remote Controller
- LE HID, Beacon,
- Home Automation
- Key fob, wristband, wearable device

2. GENERAL SPECIFICATION

General Specification	
Chipset	Realtek
Product	FSC-BT626
Dimension	13mm x 26.9mm x 2mm
Bluetooth Specification	Bluetooth V4.2 (Single Mode)
Power Supply	1.8V~3.3 Volt DC
Output Power	4 dBm
Sensitivity	-90dBm@0.1%BER
Frequency Band	2.402GHz -2.480GHz ISM band
Modulation	FHSS,GFSK,DPSK,DQPSK
Baseband Crystal OSC	40MHz , 32.768KHZ
Hopping & channels	1600hops/sec, 2MHz channel space,79 Channels
RF Input Impedance	50 ohms
Antenna	Integrated chip antenna
Interface	Data: UART, I²C,SPI
Profile	GATT(BLE Standard) MFI,Airsync,ANCS, iBeacon, OTA
Temperature	-20°C to +70 °C
Humidity	10%~95% Non-Condensing
Environmental	RoHS Compliant

Table 1

3. PHYSICAL CHARACTERISTIC

FSC-BT626 dimension is 26.9mm(L)x13mm(W)x2mm(H).

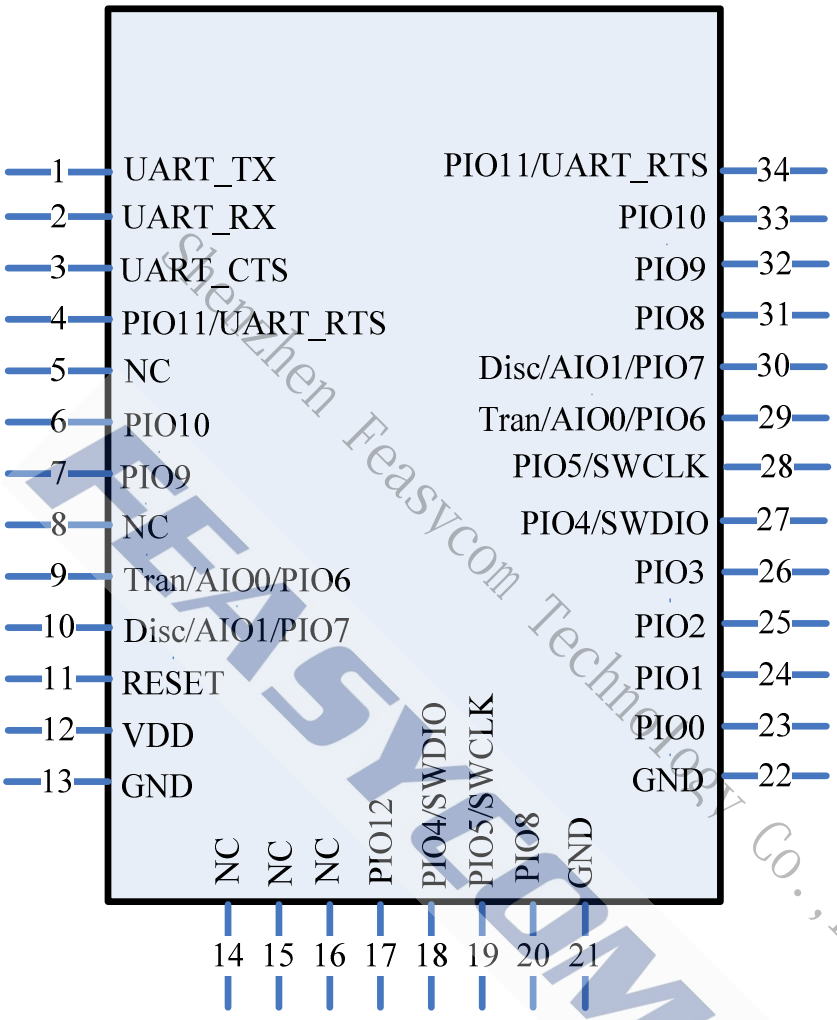

Figure2: FSC-BT626 PIN Diagram

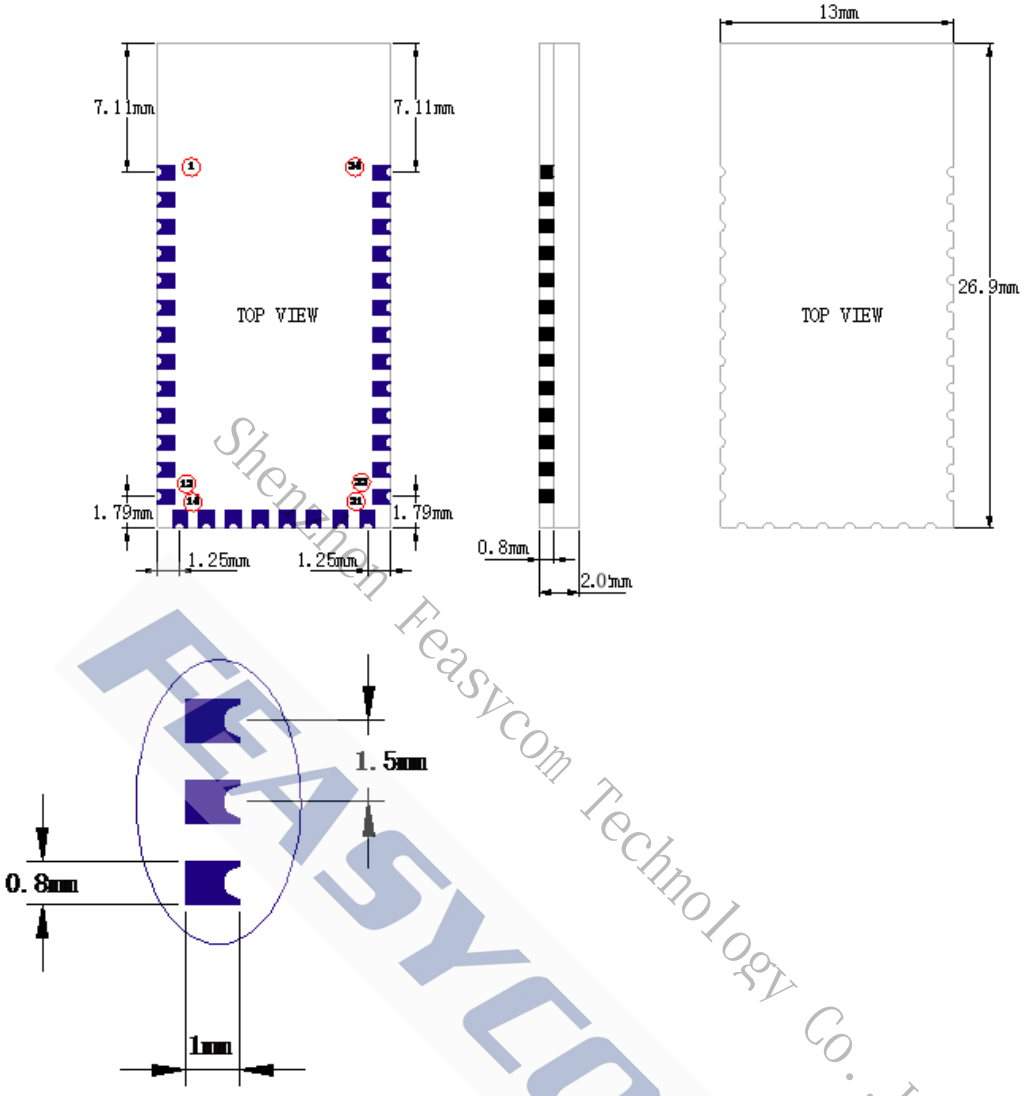

Figure 3：Package Dimensions（TOP VIEW）

4. PIN DEFINITION DESCRIPTIONS

* **Special tips:**. All I/O can be as a WAKE, besides PIO13.

Pin	Pin Name	Pad Type	Description
1	UART-TX	CMOS output	UART data output
2	UART-RX	CMOS input	UART data input
3	UART-CTS	I/O	UART clear to send active low Alternative Function: Programmable input/output line
4	PIO11/UART-RTS	I/O	UART request to send active low Alternative Function: Programmable input/output line
5	NC	NC	***NC*** ***Please have the pin dangling.***
6	Tran/AIO0/PIO6	Bi-directional	Programmable input/output line ***Pin reuse: I/O,I2C_CLK,ADC***
7	Disc/AIO1/PIO7	Bi-directional	Programmable input/output line ***Pin reuse: I/O,I2C_DAT,ADC***
8	NC	NC	***NC*** ***Please have the pin dangling.***
9	PIO10	Bi-directional	Programmable input/output line ***Pin reuse: I/O,I2C_CLK,ADC***
10	PIO9	Bi-directional	Programmable input/output line ***Pin reuse: I/O,I2C_DAT,ADC***
11	RESET	CMOS input	Reset if low. Input debounced so must be low for >5ms to cause a reset.
12	VDD	VDD	Power supply voltage 1.8V ~ 3.3V
13	GND	VSS	Power Ground
14	NC	NC	NC
15	NC	NC	NC
16	NC	NC	NC
17	PIO12	I/O	Programmable input/output line
18	PIO4/SWDIO	I/O	Programmable input/output line **Or Update Interface(SWDAT)**
19	PIO5/SWCLK	I/O	Programmable input/output line

			Or Update Interface(SWCLK)
20	PIO8	I/O	Programmable input/output line
21	GND	VSS	Power Ground
22	GND	VSS	Power Ground
23	PIO0	I/O	Programmable input/output line ***Pin reuse: SPI_CLK***
24	PIO1	I/O	Programmable input/output line ***Pin reuse: SPI_MISO***
25	PIO2	I/O	Programmable input/output line ***Pin reuse: SPI_MOSI***
26	PIO3	I/O	Programmable input/output line ***Pin reuse: SPI_CSB***
27	PIO4/SWDIO	I/O	Programmable input/output line **Or Update Interface(SWDAT)**
28	PIO5/SWCLK	I/O	Programmable input/output line **Or Update Interface(SWCLK)**
29	Tran/AIO0/PIO6	Bi-directional	Programmable input/output line ***Pin reuse: I/O,I2C_CLK,ADC***
30	Disc/AIO1/PIO7	Bi-directional	Programmable input/output line ***Pin reuse: I/O,I2C_DAT,ADC***
31	PIO8	I/O	Programmable input/output line
32	PIO9	I/O	Programmable input/output line
33	PIO10	I/O	Programmable input/output line
34	PIO11/UART-RTS	I/O	UART request to send active low Alternative Function: Programmable input/output line

Table 2

5. Interface Characteristics

5.1 UART Interface

Four signals are used to implement the UART function. When FSC-BT626 is connected to another digital device, UART_RX and UART_TX transfer data between the two devices. The remaining two signals, UART_CTS and UART_RTS, can be used to implement RS232 hardware flow control where both are active low indicators.

The interface consists of four-line connection as described in below:

Signal name	Driving source	Description
UART-TX	FSC-BT626 module	Data from FSC-BT626 module
UART-RX	Host	Data from Host
UART-RTS	FSC-BT626 module	Request to send output of FSC-BT626 module
UART-CTS	Host	Clear to send input of FSC-BT626 module

Table 3

Default Data Format

Property	Possible Values
Baud Rate	115. 2 Kbps
Flow Control	None
Data bit length	8bit
Parity	None
Number of Stop Bits	1

Table 4

5.2 I²C Interface

- Up to two I2C bus interfaces can support both master and slave mode with a frequency up to 400KHZ.
- Provide arbitration function, optional PEC(packet error checking) generation and checking.
- Supports 7 –bit and 10 –bit addressing mode and general call addressing mode.

The I2C interface is an internal circuit allowing communication with an external I2C interface which is an industry standard two line serial interface used for connection to external hardware. These two serial lines are known as a serial data line (SDA) and a serial clock line (SCL). The I2C module provides two data transfer rates: 100 kHz of standard mode or 400kHz of the fast mode. The I2C module also has an arbitration detect function to prevent the situation where more than one master attempts to transmit data to the I2C bus at the same time. A CRC-8 calculator is also provided in I2C interface to perform packet error checking for I2C data.

5.3 Analog to digital converter (ADC)

- Embed 8-CH 12-bit Sigma-Delta ADC
- Conversion range: VνSSA to VDDA (1.8 to 3.3 V)
- Temperature sensor

One 12-bit 1 μs multi-channel ADC is integrated in the device.

The conversion range is between 1.8 V < VDDA < 3.3 V. An analog watchdog block can be used to detect the channels, which are required to remain within a specific threshold window. A configurable channel management block of analog inputs also can be used to perform conversions in single, continuous, scan or discontinuous mode to support more advanced usages. The ADC can be triggered from the events generated by the general-purpose timers (TMx) and the advanced-control timers (TM1) with internal connection.

The temperature sensor can be used to generate a voltage that varies linearly with temperature. Each device is factory-calibrated to improve the accuracy and the calibration data are stored in the system memory area.

5.4 SPI Interface

Support 3wire/2wire SPI.

Up to two SPIs are able to communicate up to 18 Mbits/s in slave and master modes in full duplex and half-duplex communication modes. The 3-bit prescaler gives 8 master mode frequencies and the frame size is configurable from 4 bits to 16 bits.

Unless otherwise specified, the parameters given in Table 8 for SPI are derived from tests performed under the ambient temperature.

6. RECOMMENDED TEMPERATURE REFLOW PROFILE

The re-flow profiles are illustrated in Figure 11 and Figure 12 below.

- Follow: IPC/JEDEC J-STD-020 C
- Condition:
  - Average ramp-up rate(217℃ to peak):1~2℃/sec max.
  - Preheat:150~200C,60~180 seconds
  - Temperature maintained above 217℃:60~150 seconds
  - Time within 5℃ of actual peak temperature:20~40 sec.
  - Peak temperature:250+0/-5℃ or 260+0/-5℃
  - Ramp-down rate:3℃/sec.max.
  - Time 25℃ to peak temperature:8 minutes max
  - Cycloe interval：5 minus

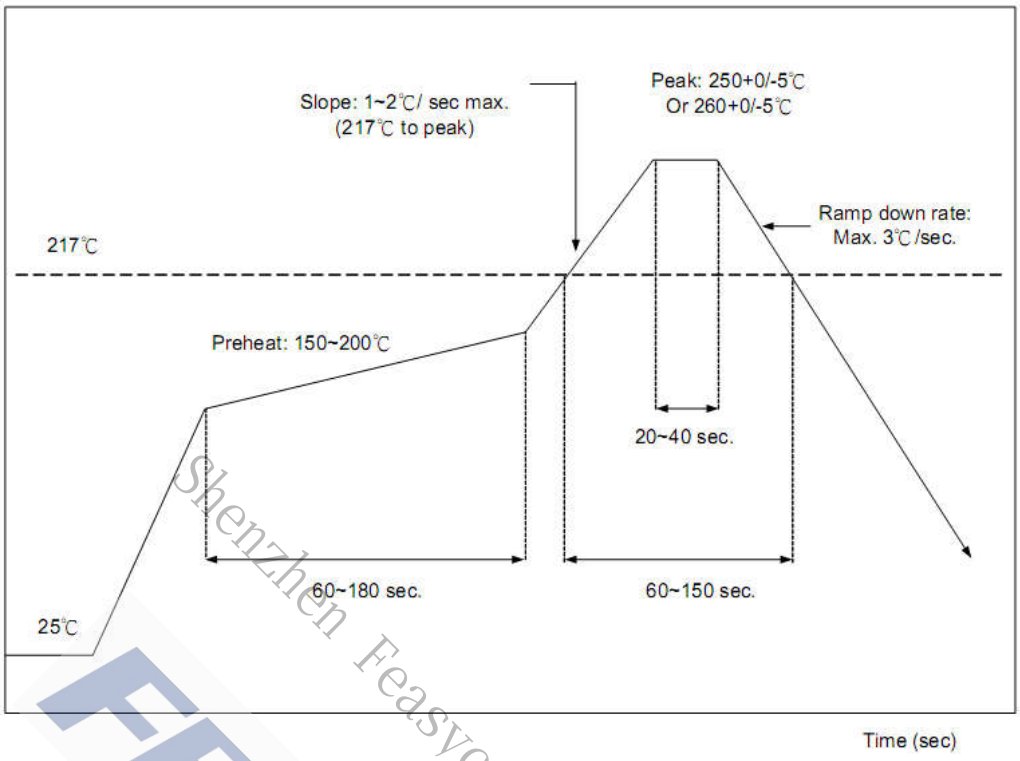

Figure 4: Typical Lead-free Re-flow Solder Profile

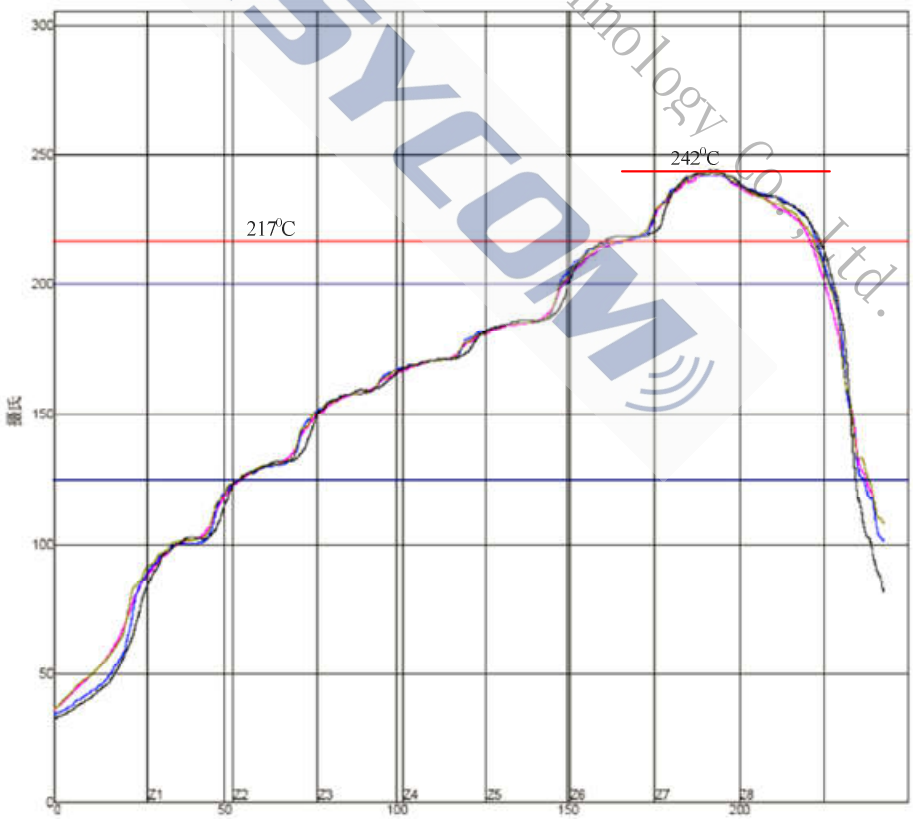

Figure 5: Typical Lead-free Re-flow

The soldering profile depends on various parameters according to the use of different solder and material. The data here is given only for guidance on solder re-flow.

FSC-BT626 will withstand up to two re-flows to a maximum temperature of 245°C.

7. Reliability and Environmental Specification

7.1 Temperature test

Put the module in demo board which uses exit power supply, power on the module and connect to mobile. Then put the demo in the －20℃ space for 1 hour and then move to +70℃ space within 1minute, after 1 hour move back to －20℃ space within1 minute. This is 1 cycle. The cycles are 32 times and the units have to pass the testing.

7.2 Vibration Test

The module is being tested without package. The displacement requests 1.5mm and sample is vibrated in three directions(X,Y,Z).Vibration frequency set as 0.5G , a sweep rate of 0.1 octave/min from 5Hz to 100Hz last for 90 minutes each direction. Vibration frequency set as 1.5G, a sweep rate of 0.25 octave/min from 100Hz to 500Hz last for 20 minutes each direction.

7.3 Desquamation test

Use clamp to fix the module, measure the pull of the component in the module, make sure the module`s soldering is good.

7.4 Drop test

Free fall the module (condition built in a wrapper which can defend ESD) from 150cm height to cement ground, each side twice, total twelve times. The appearance will not be damaged and all functions OK.

7.5 Packaging information

After unpacking, the module should be stored in environment as follows:

- Temperature: 25℃ ± 2℃
- Humidity: <60%
- No acidity, sulfur or chlorine environment

The module must be used in four days after unpacking.

8. Layout and Soldering Considerations

8.1 Soldering Recommendations

FSC-BT626 is compatible with industrial standard reflow profile for Pb-free solders. The reflow profile used is dependent on the thermal mass of the entire populated PCB, heat transfer efficiency of the oven and particular type of solder paste used. Consult the datasheet of particular solder paste for profile configurations.

Feasycom will give following recommendations for soldering the module to ensure reliable solder joint and operation of the module after soldering. Since the profile used is process and layout dependent, the optimum profile should be studied case by case. Thus following recommendation should be taken as a starting point guide.

8.2 Layout Guidelines

It is strongly recommended to use good layout practices to ensure proper operation of the module. Placing copper or any metal near antenna deteriorates its operation by having effect on the matching properties. Metal shield around the antenna will prevent the radiation and thus metal case should not be used with the module. Use grounding vias separated max 3 mm apart at the edge of grounding areas to prevent RF penetrating inside the PCB and causing an unintentional resonator. Use GND vias all around the PCB edges.

The mother board should have no bare conductors or vias in this restricted area, because it is not covered by stop mask print. Also no copper (planes, traces or vias) are allowed in this area, because of mismatching the on-board antenna.

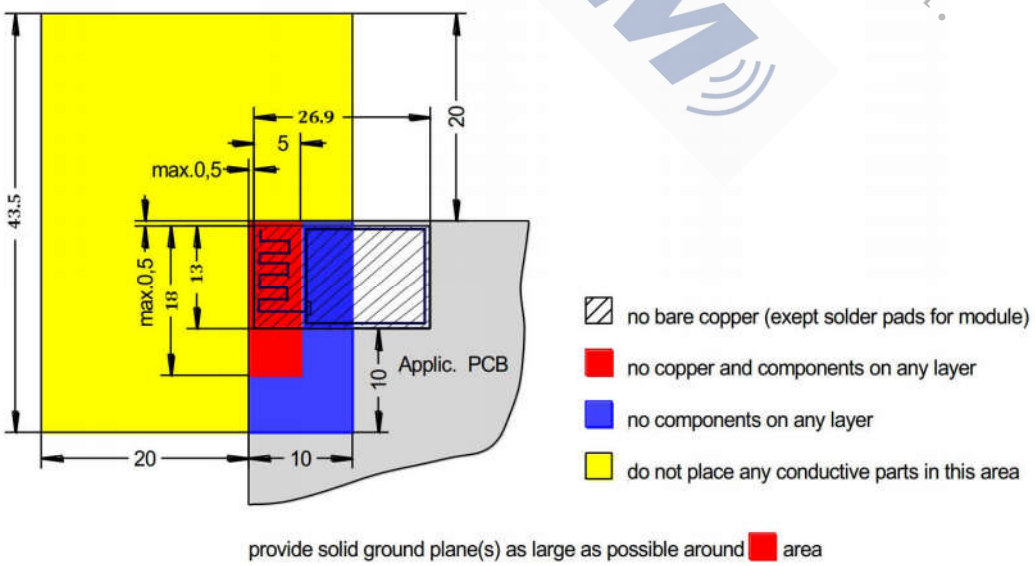

Figure 6: FSC-BT626 Restricted Area

Following recommendations helps to avoid EMC problems arising in the design. Note that each design is unique and the following list do not consider all basic design rules such as avoiding capacitive coupling between signal lines. Following list is aimed to avoid EMC problems caused by RF part of the module. Use good consideration to avoid problems arising from digital signals in the design.

Ensure that signal lines have return paths as short as possible. For example if a signal goes to an inner layer through a via, always use ground vias around it. Locate them tightly and symmetrically around the signal vias. Routing of any sensitive signals should be done in the inner layers of the PCB. Sensitive traces should have a ground area above and under the line. If this is not possible, make sure that the return path is short by other means (for example using a ground line next to the signal line).

9. Application Schematic